Notice of Allowability	Application No. 10/051,483	Applicant(s) JOO ET AL.	
	Examiner Jason M. Perilla	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed March 17, 2006*.

2. ☒ The allowed claim(s) is/are *1-4, 6-21, 23-26, 28-45, 47, 48, 50, 51, 53-57, and 60-62 renumbered respectively as claims 1-54*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20060410* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. 1-4, 6-21, 23-26, 28-45, 47, 48, 50, 51, 53-57, and 60-65 are pending in the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Kimton N. Eng on April 11, 2006.

The application has been amended as follows wherein the following versions of claims 1, 6, 7, 10, 12, 14, 16, 17, 19, 21, 24-26, 30, 32, 34, 36, 37, 39, 40, 42, 44, 45, 48, 51, 53-55, 57, 60, 61 replace all prior versions in their entirety, and claims 63-65 are cancelled.

1. A clock synchronization circuit adapted to receive an input clock signal and adapted to receive current data signals and respective future data signals, the clock synchronization circuit comprising:

a logic circuit coupled to receive the future data and current data signals, and operable to develop a plurality of phase shift control signals in response to the future data and current data signals; and

a phase shift circuit adapted to receive the input clock signal and coupled to the logic circuit to receive the plurality of phase shift control signals, and operable to generate a phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the current and respective future data signals ~~responsive to the input clock signal~~, the phase shifted clock signal having a delay determined by the plurality of phase shift control signals.

6. The clock synchronization circuit of claim 1 wherein the logic circuit comprises a plurality of XNOR gates, each XNOR gate receiving a ~~respective future~~ current data signal and ~~the~~ its respective future ~~corresponding current~~ data signal and developing a corresponding one of the plurality of phase shift control signals responsive to the future data and current data signals.

7. The clock synchronization circuit of claim 1 wherein the phase shift circuit comprises:

a plurality of switching circuits coupled to an output node, each switching circuit coupled to the logic circuit to receive a respective one of the plurality of phase shift control signals and operable responsive to the respective one of the plurality of phase shift control signal having a first state to couple a first phase shift element to the output node and operable responsive to the respective one of the phase shift control signal having a second state to couple a second phase shift element to the output node;

an input circuit having an input adapted to receive the input clock signal and having an output coupled to the output node, and being operable to develop a charging signal on the output node responsive to the input clock signal, the charging signal having a delay in reaching a threshold value that is determined by the first and second phase shift elements coupled to the output node; and

an output circuit coupled to the output node and operable to develop the phase shifted clock signal responsive to the charging signal reaching the threshold value.

10. The clock synchronization circuit of claim 9 wherein each of the plurality of switching circuits comprises a first transistor coupled in series with the corresponding first capacitor between the output node and a reference voltage source, and further comprises a second transistor coupled in series with the corresponding second capacitor between the output node and the reference voltage source, the first and second transistors of each of the plurality of switching circuits each ~~transistor~~ having a control terminal coupled to receive the ~~corresponding~~ phase shift control signal of its particular switching circuit.

12. The clock synchronization circuit of claim ~~5~~ 1 wherein the phase shift circuit comprises:

an input circuit adapted to receive the input clock signal and being operable to develop an output signal on an output responsive to the input clock signal;

an output circuit having an input coupled to a charging node and being operable to develop the phase shifted clock signal responsive to a charging signal on the charging node reaching a threshold value; and

a plurality of switching circuits coupled in series between the output of the input circuit and the charging node; each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to ~~the~~ its respective phase shift control signal having a first state to provide a first phase shift element and operable responsive to ~~the~~ its respective phase shift control signal having a second state to provide a second phase shift element, the combination of first and second phase shift elements coupled in series controlling a rate at which the charging signal reaches the threshold value.

14. The clock synchronization circuit of claim 12 wherein each first phase shift element comprises a resistor and each second phase shift element comprises a transistor having signal terminals coupled in parallel with ~~the~~ its corresponding resistor and having a control terminal coupled to receive ~~the~~ its corresponding phase shift control signal.

16. The clock synchronization circuit of claim ~~5~~ 1 wherein the ~~delay~~ phase shift circuit comprises:

an input circuit adapted to receive the input clock signal and including a supply node, the input circuit operable to develop the phase shifted clock signal responsive to the input clock signal, the phase shift of the phase shifted clock signal being a function of a supply current provided to the supply node; and

a plurality of switching circuits coupled in parallel between a supply voltage source and the supply node, each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to its respective ~~the~~ phase shift control signal having a first state to provide a first current to the supply node and operable responsive to its respective ~~the~~ phase shift control signal having a second state to provide a second current to the supply node, the combination of first and second currents from the plurality of switching circuits controlling the supply current provided to the supply node.

17. The clock synchronization circuit of claim 16 wherein each switching circuit comprises a transistor having signal terminals coupled between the supply voltage source and the supply node, and having a control terminal coupled to receive ~~the~~ its corresponding ~~delay~~ phase shift control signal.

19. The clock synchronization circuit of claim 16 wherein the input circuit comprises a first inverter coupled to receive the input clock signal and including the supply node, and a second inverter coupled in series with the first inverter and operable to develop the phase shifted ~~delayed~~ clock signal responsive to an output signal from first inverter.

21. A data output circuit, comprising:

a plurality of data drivers, each data driver adapted to receive a respective read data signal and being operable to store the respective read data signal in response to a phase shifted clock signal and output the stored respective read data signal as a corresponding output data signal; and

a clock synchronization circuit adapted to receive an input clock signal and adapted to receive the plurality of respective read and corresponding output data signals, and coupled to the plurality of data drivers, the clock synchronization circuit operable to generate ~~a~~ the phase shifted clock signal in response to the input clock signal and apply the phase shifted clock signal to clock the plurality of respective read data signals out of the plurality of data drivers as the corresponding plurality of output data signals, the clock synchronization circuit operable to ~~operable to~~ add a first phase shift increment to the phase shift of the phase shifted clock signal for each of the plurality of read data signals and corresponding output data signals having the same logic state, and operable to alternatively add a second phase shift increment to the phase shift of the phase shifted clock signal for each of the plurality of read data signals and corresponding output data signals having complementary logic states.

24. The data output circuit of claim 21 wherein the phase shift of the phase shifted clock signal comprises a phase shift having a value that is a function of the logic states of the plurality of respective read data and corresponding output data signals.

25. A data output circuit, comprising:

a plurality of data drivers, each data driver adapted to receive a respective read data signal and being operable to store the respective read data signal in response to a phase shifted clock signal and output the stored respective read data signal as a corresponding output data signal;

a logic circuit coupled to receive the plurality of respective read data and ~~the~~ corresponding output data signals, and operable to develop a plurality of phase shift control signals in response to the plurality of respective read data and ~~the~~ corresponding output data signals;

a plurality of switching circuits coupled to an output node, each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to the respective one of the phase shift control signal having a first state to couple a respective first delay element to the output node and operable responsive to the respective one of the phase shift control signals having a second state to couple a respective second delay element to the output node;

an input circuit having an input adapted to receive an input clock signal and having an output coupled to the output node, and being operable to develop a charging signal on the output node responsive to the input clock signal, the charging signal having a delay in reaching a threshold value that is determined by the first and second delay elements coupled to the output node; and

an output circuit coupled to the output node and operable to develop the phase shift clock signal responsive to the charging signal reaching the threshold value.

26. The data output circuit of claim 25 wherein the logic circuit comprises a plurality of XNOR gates, each XNOR gate receiving one of the plurality of respective read data and corresponding output data signals and developing a corresponding one of the plurality of phase shift control signals responsive to the one of the plurality of respective read data and corresponding output data signals.

30. The data output circuit of claim 29 wherein each of the plurality of switching circuits comprises a first transistor coupled in series with the respective first capacitor between the output node and a reference voltage source, and further comprises a second transistor coupled in series with the respective second capacitor between the output node and the reference voltage source, the first and second transistors of each of the plurality of switching circuits each ~~transistor~~ having a control terminal coupled to receive the ~~corresponding~~ phase shift control signal of its particular switching circuit.

32. ~~The~~ A data output circuit comprising ~~of claim 25 wherein the phase shift circuit comprises~~:

a plurality of data drivers, each data driver adapted to receive a respective read data signal and being operable to store the respective read data signal in response to a phase shifted clock signal and output the stored respective read data signal as a corresponding output data signal;

a logic circuit coupled to receive the plurality of respective read data and corresponding output data signals, and operable to develop a plurality of phase shift control signals in response to the plurality of respective read data and corresponding output data signals;

an input circuit adapted to receive an ~~the~~ input clock signal and being operable to develop an output signal on an output responsive to the input clock signal;

an output circuit having an input coupled to a charging node and being operable to develop the phase shifted clock signal responsive to a charging signal on the charging node reaching a threshold value; and

a plurality of switching circuits coupled in series between the output of the input circuit and the charging node; each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to its respective ~~the~~ phase shift control signal having a first state to provide a first delay element and operable responsive to its respective ~~the~~ phase shift control signal having a second state to provide a second delay element, the combination of first and second delay elements coupled in series controlling a rate at which the charging signal reaches the threshold value.

34. The data output circuit of claim 32 wherein each first delay element comprises a resistor and each second delay element comprises a transistor having signal terminals coupled in parallel with ~~the~~ its corresponding resistor and having a control terminal coupled to receive ~~the~~ its corresponding phase shift control signal.

36. ~~The~~ A data output circuit comprising ~~of claim 25 wherein the phase shift circuit comprises~~:

a plurality of data drivers, each data driver adapted to receive a respective read data signal and being operable to store the respective read data signal in response to a phase shifted clock signal and output the stored respective read data signal as a corresponding output data signal;

a logic circuit coupled to receive the plurality of respective read data and corresponding output data signals, and operable to develop a plurality of phase shift control signals in response to the plurality of respective read data and corresponding output data signals;

an input circuit adapted to receive an ~~the~~ input clock signal and including a ~~ground~~ supply node, the input circuit operable to develop the phase shifted clock signal responsive to the input clock signal, the phase shift of the phase shifted clock signal being a function of a supply current provided to the supply node; and

a plurality of switching circuits coupled in parallel between a ground voltage source and the ~~ground~~ supply node, each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to its respective ~~the~~ phase shift control signal having a first state to provide a first current to the supply node and operable responsive to its respective ~~the~~ phase shift control signal having a second state to provide a second current to the ~~ground~~ supply node, the combination of first and second currents from the plurality of switching circuits controlling the sink current provided to the ~~ground~~ supply node.

37. The data output circuit of claim 36 wherein each switching circuit comprises a transistor having signal terminals coupled between the ground voltage source and the supply ~~ground~~ node, and having a control terminal coupled to receive ~~the~~ its corresponding phase shift control signal, and ~~one~~ an additional switching circuit comprises a transistor having signal terminals coupled between the ground voltage source and the ~~ground~~ supply node and having a control terminal adapted to receive a bias voltage.

39. The data output circuit of claim 36 wherein the input circuit comprises a first inverter coupled to receive the input clock signal and including the ~~ground~~ supply node, and a second inverter coupled in series with the first inverter and operable to develop the delayed clock signal responsive to an output signal from first inverter.

40. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a clock synchronization circuit adapted to receive an input clock and coupled to the read/write circuit to receive current data signals and respective future data signals, the clock synchronization circuit comprising:

a logic circuit coupled to receive the future data and current data signals, and operable to develop a plurality of phase shift control signals in response to the future data and current data signals; and

a phase shift circuit adapted to receive the input clock signal and coupled to the logic circuit to receive the plurality of phase shift control signals, and operable to generate a phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the current and future data signals ~~responsive to the input clock signal~~, the phase shifted clock signal having a delay determined by the plurality of phase shift control signals, and the phase shifted clock signal being applied to data drivers in the read/write circuit to clock data onto the data bus.

42. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a clock synchronization circuit adapted to receive an input clock and coupled to the read/write circuit to receive current data signals and respective future data signals, the clock synchronization circuit comprising:

a logic circuit coupled to receive the future data and current data signals, and operable to develop a plurality of phase shift control signals in response to the future data and current data signals; and

a phase shift circuit adapted to receive the input clock signal and coupled to the logic circuit to receive the plurality of phase shift control signals, and operable to generate a phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the current and future data signals ~~responsive to the input clock signal~~, the phase shifted clock signal having a delay determined by the plurality of phase shift control signals, and the phase shifted clock signal being applied to data drivers in the read/write circuit to clock data onto the data bus.

44. A method of providing a plurality of data signals out of an integrated circuit in synchronism with a clock signal applied to the integrated circuit, the method comprising:

detecting a respective first logic state of each of the plurality of data signals;

detecting a respective second logic state of each of the plurality of data signals;

determining an output delay from the plurality of detected respective first and second logic states; and

adjusting a delay interval relative to a transition of the clock signal based on the determination by adding a first delay increment to the output delay for each corresponding pair of detected respective first and second logic states of each data signal where the detected respective first and second logic states are equal, and adding a second delay increment to the output delay for each corresponding pair of detected respective first and second logic states of each data signal where the detected respective first and second logic states are unequal; and

outputting the plurality of data signals having the second logic state from the integrated circuit in response to the adjusted delay interval.

45. The method of claim 44 wherein the respective first logic state of each of the plurality of data signals comprises a current logic state and wherein the respective second logic state of each of the plurality of data signals comprises an upcoming logic state ~~of the data signal~~.

48. A method of delaying a plurality of data signals relative to a clock signal, comprising:

detecting a respective current logic state of each of the plurality of data signals;

detecting a respective future logic state of each of the plurality of data signals;

determining an output delay having a value that is a function of the plurality of detected respective current and future logic states for each data signal; and

delaying the plurality of data signals ~~having the future logic state~~ by the determined output delay relative to the clock signal by adding a first delay increment to the output delay for each corresponding pair of respective current and future logic states of each data signal where the detected respective current and future logic states are equal, and adding a second delay increment to the output delay for each corresponding pair of respective current and future logic states of each data signal where the detected respective current and future logic states are unequal.

51. A method of providing a plurality of data signals out of an integrated circuit, the method comprising:

detecting respective current and future logic states for each of the plurality of data signals, ~~each~~ the plurality of data signals having ~~the~~ their respective current logic states having a phase shift relative to a clock signal;

adjusting the value of the phase shift as a function of ~~the~~ a number of the plurality of data signals for which the values of ~~the~~ their respective current and future logic states are equal and adjusting the value of the phase shift as a function of ~~the~~ a number of the plurality of data signals for which ~~the~~ their respective current and future logic states are unequal; and

outputting the respective future logic state for each of the plurality of data signals, with each of the plurality of data signals having ~~the~~ its respective future logic state being phase shifted by the adjusted value of the phase shift.

53. The method of claim 51 wherein adjusting the value of the phase shift as a function of the number of the plurality of data signals for which the values of ~~the~~ their current and future logic states are unequal comprises decreasing a delay for each of the plurality of data signals for which the values of ~~the~~ their current and future logic states are unequal.

54. The method of claim 53 wherein adjusting the value of the phase shift as a function of the number of the plurality of data signals for which the values of ~~the~~ their current and future logic states are equal comprises increasing a delay for each the plurality of data signals for which the values of ~~the~~ their current and future logic states are equal.

55. The method of claim ~~52~~ 51 wherein adjusting the value of the phase shift as function of the number of the plurality of data signals for which the values of ~~the~~ their current and future logic states are unequal comprises adding a first delay increment to the phase shift ~~for each such data signal~~, and wherein adjusting the value of the phase shift as function of the number of the plurality of data signals for which the values of ~~the~~ their current and future logic states are equal comprises adding a second delay increment to the phase shift ~~for each such data signal~~.

57. A method of providing a plurality of data signals out of an integrated circuit in synchronism with a clock signal applied to the integrated circuit, the method comprising:

detecting a respective current logic state of each of the plurality of data signals;

detecting a respective upcoming logic state of each of the plurality of data signals;

for each of the plurality of data signals, ~~defining a group of data signals associated with the data signal,~~ comparing ~~the~~ their current and future logic states ~~of the data signals in the~~

~~group of data signals~~, and adjusting ~~the~~ an output delay of the plurality of data signals as a function of the current and future logic states~~ of the data signals in the group of data signals~~; and

for each of the plurality of data signals, outputting the ~~data signal having the~~ second logic states in accordance with the determination of the ~~respective~~ output delay ~~for each data signal from the integrated circuit~~.

60. The method of claim 57 wherein ~~each group~~ the plurality of data signals includes four data signals.

61. The method of claim 60 wherein adjusting the output delay of the plurality of data signals as a function of the current and future logic states of the plurality of data signals ~~in the group~~ comprises adjusting the output delay to a first value when the current and future logic states of all data signals ~~in the group~~ are equal, adjusting the output delay to a second value when the current and future logic states of one of the plurality of data signals ~~in the group~~ is changing, adjusting the output delay to a third value when the current and future logic states of two of the plurality of data signals ~~in the group~~ are changing, and adjusting the output delay to a fourth value when the current and future logic states of more than two of the plurality of data signals ~~in the group~~ are changing.

63. (Cancelled)

64. (Cancelled)

65. (Cancelled)

Claims 1-4, 6-21, 23-26, 28-45, 47, 48, 50, 51, 53-57, and 60-62 are renumbered respectively as claims 1-54, and the claim dependency is renamed accordingly.

Allowable Subject Matter

3. The following is an examiner's statement of reasons for allowance:

Claims 1-4, 6-21, 23-26, 28-45, 47, 48, 50, 51, 53-57, and 60-62 renumbered respectively as claims 1-54 are allowed because the prior art of record does not disclose or obviate phase shifting a clock signal according to a difference between current and future states of a data signal wherein the phase shifted clock signal is used to latch future data into current data.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
April 10, 2006

jmp

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER